MWA has 64 Receiver Nodes
Principle Function of each node

16 x 32 MHz digitized output

16 x 300 MHz RF input

5 Gb/s /Node
... care and feeding ...

• Power to node and tiles
• Instructions/updates to node and tiles
• Monitor health of node and tiles...
• Environmental protection
  • Weather: heat, moisture,...
  • Radio frequency interference...
A Significant complexity…

looking to measure “correlation coefficients”

• cross talk
• coupling
• common mode signal
• DC term (ED jargon)

Solved by
Phase-switching

Cycle through 16 orthogonal Walsh states…
Who?

ANU:
• Mark Waterson - WP Manager
• Errol Kowald
• Annino Vaccarella
• (Glen Torr)
• (Jonathon Kocz)
• Frank Briggs

RRI:
• Anish Roshi - RRI coordinator
• Prabu
• Srivani
• Gopal Krishna
**Receiver Node principal components**

- **16 x 300MHz analog input**
- **8 Tiles + Beamformers**
- **A/D PFB 8 inputs**
- **Backplane**
- **Aggregation Formatting**
- **Local M&C**
- **Analog Signal Conditioning**
- **Clock distribution**
- **16 x 32 MHz dig-output**
- **Correlator**
- **Station Clock**
- **Master M&C**
Analog Passband Filters and Amplifiers to adjust Power Levels

Tiles + Beamformers

Analog Signal Conditioning

A/D PFB

Clock distribution

Backplane

Aggregation Formatting

Correlator

Station Clock

Master M&C

local m&c
High-speed Digital components and synchronization
Sampling clock @660 MHz, plus Synchronization

Tiles + Beamformers

A/D PFB 8 inputs

Aggregation Formatting

Backplane

Correlator

Custom clock Module

Clock distribution

Station Clock

Analog Signal Conditioning

Clock distribution

Master M&C

Master M&C
Projected Schedule for Receiver Development…

ANU
• core electronics for 1 receiver by 1 September (w/o AgFo)
• 4 receivers in Q4 2007
• packaging by 1 January

RRI
• simulation of 2xPFB code with ADC interface - end June
• 1 channel ADFB board - early July
• code ready for serial data output - early July
• schematic for AgFo board - end July
• 4 channel ADFB board - early August
• PCB fabrication of AgFo board - end August
• most code ready for node - early September
• 2 fully populated boards - mid September
• testing of AgFo board - mid September
• high-speed digital components ready at RRI - mid October
Analog Passband Filters and Amplifiers to adjust Power Levels
Prototype Passband Filters: shipped 2 to WA for 1T expts (no amplifiers)
M&C ... <=> ... ASC units
CSIRO ICT Board: (4 chan of 1 GHz bandwidth)

CSIRO Board... not ours!
CSIRO Gbit Wireless Board: (4 chan of 1 GHz bandwidth)
CSIRO Board: (Reconfigured to 8 input channels of 500 MHz)

Connection To back plane

2 X 32 Msamp/s X (2x4 bit cmplx)

FPGA

2 X 660 Msamp/s X 8 bit

A/D

2 X (0 - 330 MHz analog)
CSIRO Board: (Reconfigurable to 8 input channels of 500 MHz)

PFB Codes …running in development board
- modified Berkeley PFB from Ludi
- ATNF PFB from Grant

Prototype board…
- partially populated with ADC and FPGA in 1 channel
- shipped to RRI
Overall Receiver Mode/State Transitions

(Mark Waterson)

Data:
- Power-on sequence/delays
- Which BF's get turned on
- Temps/volts (ok/warn/fail)
- FPGA code blocks

Data:
- BF Phase switch table
- ASC initial atten values
- NTP time to start/ARM
- SCTN
State Diagram (Anish)

Figure 3: State machine in the ADFB board FPGAs
3. Milestones Crossed

- Block diagram level design of AgFo ready for discussion

- Block diagram of clock and synchronization requirements for Receiver Node ready for discussion

- Block diagram level design of ADFB firmware ready for discussion

- Simulation of two (Grant’s) PFBs + ADC interface is being done; preliminary results on the resource utilization and clock speed are available

- Requirements of the Analog system in the Receiver Node has been worked out and ready for discussion
Projected Schedule for Receiver Development…

ANU
• core electronics for 1 receiver by 1 September (w/o AgFo)
• 4 receivers in Q4 2007
• packaging by 1 January

RRI
• simulation of 2xPFB code with ADC interface - end June
• 1 channel ADFB board - early July
• code ready for serial data output - early July
• schematic for AgFo board - end July
• 4 channel ADFB board - early August
• PCB fabrication of AgFo board - end August
• most code ready for node - early September
• 2 fully populated boards - mid September
• testing of AgFo board - mid September
• high-speed digital components ready at RRI - mid October