Clock workpackage

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Current status

- Specifications complete
- Conceptual design complete
- Engineering design not complete
- Engineering resources not identified
Conceptual design

Three components:

- **Reference clock** \[commercial, readily available\]
- Electrical to 64 optical signals
  - Epoch signal encoding
- Node hardware on receiver Agfo board
  - Optical to electrical
  - Epoch signal decode and regeneration
  - Clean-up loop
  - Up-convert and distribute

Requires a fibre from central building to each node
Not yet determined

- Epoch signal frequency
- Main reference frequency
Major issue

- Finding engineering support
Other issues

• Approach to implementing delay adjustment
• Timing noise inherent in tranceivers (may not been given in data sheets)