Receiver Function:

RF
0-300 MHz

Digital
25 x 1.5 MHz
= 32 MHz
Receiver Function:

RF $ightarrow$ 0-300 MHz $ightarrow$ Digital

$25 \times 1.5 \text{ MHz} = 32 \text{ MHz}$

Channel Width = $F_{\text{oversamp}} \times \frac{660\text{MHz}}{2 \times 256} = 1.5 \text{ MHz}$

Spacing = $\frac{660\text{MHz}}{2 \times 256} = 1.3 \text{ MHz}$
Receiver Interfaces [WPs]:

- Antennas
- Transport Layer/Correlator
- Monitor & Control
- Infrastructure
- Clock
Receiver Interfaces [WPs]:

- RF Power
- Beamformer Cntl
- Phase Switching

: Power/voltage levels, Impedences, Cables, Connectors, Protocols ...
Receiver Interfaces [WPs]:

- Power, voltages, ...
- comms, fibres, RF cables
- conduits
- physical location?
  - surface, hole in ground
- heat/coolant transport
Receiver Interfaces [WPs]:

- Fibre Bundle
- Monitor & Control
- Transport Layer/Relator
- Clock
Receiver Interfaces [WPs]:

- Clock “module” for Node
- Sampling Clock 660MHz (?)
- SCTN signal
- Phase Switching coordination for Tiles
Receiver Interfaces [WPs]:

- Hardware compatibility
- Protocols
- Data rates
- Formats

Distances... <= array config & location of correlator, etc.
Receiver Interfaces [WPs]:

- to/from Tiles
- to/from Receiver
  - Gains
  - Channel Selection
  - Mode selection

Monitor & Control
32T / Prototyping Layout!

Receiver Node principal components

Tiles + Beamformers

A/D PFB 8 inputs

Analog Signal Conditioning

Clock distribution

Power distribution

Local M&C

Master M&C

Correlator

Station Clock
Mark Waterson (ANU) Murray Dawson (ANU)

- System layout/design
- packaging/integration
- environmental issues
Glen Torr (ANU/ADFA)
Gain control, BW limit
- cheap ICs
- serial I²C interface
- Individually boxed
- avoid connectors (?)
John Bunton ++ (CSIRO/ATNF) (Joseph, Ludi, …)
“ICT Boards”
• prototypes exist at CSIRO
• need Firmware… exploit xNTD compatibilities
• (USB control…)
• evolve with xNTD for 500T ?
Receiver Node principal components

32T / Prototyping Layout!

? Needs Specifications to Correlator/Transport Layer?
(ANU+, ATNF/CSIRO, Domain46)

• 500T… integrate into the A/D+PFB board
Annino Vaccarella (ANU)
- Single Board Computer PC104
- 8 serial ports to Tile BFs
- I²C interface to ASC units
- 2 fibres from bundle to central M&C
- (USB to high speed dig.)

M&C Tasks:
- tile-BF, pointing...
- mode/channel selection
- monitor/set gains
- general health status
Receiver Node principal components

- Tiles + Beamformers
- A/D PFB 8 inputs
- Backplane
- Aggregation Formatting
- Clock distribution
- Power distribution
- Master M&C
- Correlator
- Station Clock

? ANU, ATNF/CSIRO, Haystack?
- not considered novel/tough
- need to locate capability & resource it…
Node & Receiver timeline

• modularizable…
• but, needs ~ FTE year
• ASCs, m&c … OK
• ICT digital boards… firmware is lacking
• RSAA electronics pre-booked until mid-year
Node & Receiver timeline

- modularizable…
- but, needs ~ FTE year
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Pick any 2!
Node & Receiver timeline

• modularizable…
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• ASCs, m&c … OK
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• If must be fast, then needs more resource…
Node & Receiver timeline

• modularizable…
• but, needs ~ FTE year
• ASCs, m&c … OK
• ICT digital boards… firmware is lacking
• RSAA electronics pre-booked until mid-year

• If must be fast, then needs more resource…

• or not-so-good…
  -? Start with 8T, put “unpackaged” Node unit in caravan?
Node & Receiver cost uncertainty

- cost of FPGA chips… !
  \[ 9 \times $500 \times 64 = $0.3M \]