e2e Integration & Testing

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Purpose

- To establish an end-to-end pathway in the laboratory, verify that subsystems are correctly interfaced, and that the system overall meets the performance specifications
Digital Subsystem Goals

- verify correct electrical performance in the following 3 interfaces:
  - AgFo - PFB
  - PFB - CB
  - CB - RTC

- verify that, in the normal operating state, test packets are received correctly across all 3 interfaces:
  - AgFo - PFB
  - PFB - CB
  - CB - RTC
32T Signal Flow Block Diagram

- 32 tiles
- 32 beamformers
- 4 receivers
- 1 PFB and PFB/RTM
- 1 CB and CB/RTM
- 1 RTC stand-in
32T Digital Architecture
Software Simulation

- C programs to simulate and inter-compare to the bit level:
  - Receiver (AgFo) output
  - PFB board
  - CB board
  - RTC packet capture
- recsim & VHDL module generate:
  - constant frequency tone
  - frequency sweep
  - pseudo-random sequence
Test Setup at Haystack

- Single path from dipole through RTC
- Mark Waterson at Haystack last week to integrate DOC with receiver code
Integration Data Path
Receiver to Polyphase Filterbank Board

- optical signal at 1.72 Gb/s
- physical link integrity using Xilinx’s Chipscope
- received packets in PFB examined using “Ludiscope”
- so far, only spot-checking of AgFo data has been done, but plan is to use generator module in the AgFo to send the prs
Polyphase Filterbank Board to Correlator Board

- correlator internal interconnection
- 2.0 Gb/s per twisted pair
- physical verified via Chipscope BER test set
- PFB packets captured on CB using Ludiscope and spot-checked
Correlator Board to Real Time Computer

- correlator output packets (with sequential count as contents) verified by capture with the Wireshark packet-sniffer on RTC surrogate

- haven’t yet done extensive pattern intercomparisons using rtcsim

- will interface with RTC from CfA some time in the next few weeks
Plans

- Anish Roshi and Prabu Thiagaraj at Haystack next week
  - plan to inject analog signals into receiver and process as far as possible through system
  - requires RRI clock setup
  - ideally will achieve a cross-correlation; absent that, a post pfb detection
- will test complete digital chain by generating test waveforms in AgFo board and passing them all the way through the system to RTC capture (will eventually form part of stand-alone test suite)